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Description

METHOD FOR PATTERNING HFO2-CONTAINING DIELECTRIC

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a method for patterning an HfO2-containing dielectric, and more particularly, to a method for patterning an HfO2-containing gate dielectric without damaging STI positioned on the same wafer.

[0003] 2. Description of the Prior Art

[0004] For realizing the low power MOS transistor at the 65nm node and beyond, it is necessary to reduce the gate leakage current for thinner gate dielectrics. The introduction of high-k gate material would be advantageous for extending current MOS technology. After several years of work, many research groups are now focusing on hafnium (Hf) based material and are evaluating the natural of these materials extensively. Among the considerable Hf-based

materials, HfO2 is often evaluated to be combined into a metal gate structure.

[0005] However, HfO2-containing dielectric (including HfO2, HfSiO, HfSiON, HfAlO, and so on) is known for more difficult to be pattern etched comparing to SiO2 based dielectric. The conventional method of etching the HfO2-containing dielectric involves using a strong acid, such as 49% HF solution. When using the 49% HF solution to etch the HfO2-containing dielectric, a SiO2 layer, such as a shallow trench isolation (STI) layer, will be also removed. Furthermore, the etching rate of the SiO2 layer is much higher than that of the HfO2-containing dielectric, and the SiO2 layer will be seriously damaged while patterning the HfO2-containing dielectric.

[0006] Another conventional method of etching the HfO2-containing dielectric is using a high insert gas plasma with more than 60% Ar. The insert gas plasma has no selectivity while etching, and may also result in the SiO2 layer being damaged during over-etch.

[0007] Please refer to Figs. 1 and 2, which show a conventional etching process of the HfO2-containing dielectric. An STI layer 18 is formed on a wafer 10, and an HfO2-containing gate dielectric 12 covers the wafer 10 and the STI layer

18. A gate electrode 16 is formed on the HfO2-containing gate dielectric 12, and two spacers 14 are formed beside the gate electrode 16. As shown in Fig. 2, the conventional etching process such as using the strong acid or the insert gas plasma is performed to remove portions of the HfO2-containing gate dielectric 12. The etching selectively between the HfO2-containing gate dielectric 12 and the STI layer 18 is too low to bring serious damages atop the STI layer 18. As a result, the isolation effect of the STI layer 18 is reduced.

SUMMARY OF INVENTION

[0008] It is therefore a primary objective of the claimed invention to provide a method for patterning the HfO2-containing gate dielectric without damaging the SiO2 layer to solve the above-mentioned problem.

[0009] According to the claimed invention, a method for patterning an HfO2-containing gate dielectric comprises providing a wafer having a trench, a STI layer formed in the trench, the HfO2-containing gate dielectric covering the wafer and the STI layer, a gate electrode formed on the HfO2-containing gate dielectric, and at least a spacer formed beside the gate electrode. Following that, the wafer is preheated and a bromine-rich gas plasma is pro-

vided to remove portions of the HfO2-containing gate dielectric.

[0010] According to the claimed invention, a method for patterning an HfO2-containing gate dielectric comprises providing a wafer having a trench, a STI layer formed in the trench, the HfO2-containing gate dielectric covering the wafer and the STI layer, a gate electrode formed on the HfO2-containing gate dielectric, and at least a spacer formed beside the gate electrode. Following that, a nitrogen ion bombardment is used to convert the exposed HfO2-containing gate dielectric to a Hf3N4 layer. A phosphoric acid is used to remove the Hf3N4 layer.

[0011] It is an advantage of the claimed invention that the bromine-rich gas plasma has a high selectivity between the HfO2-containingdielectric and the SiO2 layer, so that the HfO2-containingdielectric can be etched without damaging the SiO2 layer.

[0012] It is another advantage of the claimed invention that the nitrogen ion bombardment can convert the HfO2-containingdielectric to the Hf3N4 layer and the phosphoric acid has a high selectivity between the Hf3N4 and SiO2 layers, so that the HfO2-containingdielectric can be etched without damaging the SiO2 layers.

[0013] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0014] Fig. 1 is a schematic diagram of a wafer before performing a gate dielectric patterning process thereon according to the prior art;

[0015] Fig. 2 is a schematic diagram of a wafer after performing a gate dielectric patterning process thereon according to the prior art;

[0016] Fig. 3 is a schematic diagram of a wafer after performing a gate dielectric patterning process thereon according to the present invention; and

[0017] Fig. 4 is a schematic diagram of a wafer after performing a gate dielectric patterning process thereon according to a second embodiment of the present invention.

Detailed Description

[0018] Please refer to Fig. 3, which shows a result of performing a patterning process according to a first embodiment of the present invention. In the first embodiment of the

present invention, a bromine-rich gas plasma is utilized to accomplish the requirement of etching the HfO2-containing dielectric with a high selectivity. In this embodiment, a MOS transistor fabrication is used to explain the present invention. Before the etching process, the half-manufactured wafer is similar to that of the prior art as shown in Fig. 1. For example, the STI layer 18 is formed on the wafer 10, and the HfO2-containing gate dielectric 12 covers the wafer 10 and the STI layer 18. The gate electrode 16 is formed on the HfO2-containing gate dielectric 12, and two spacers 14 are formed beside the gate electrode 16. The STI layer 18 and the spacer 14 may be formed of SiO2, and the gate electrode 16 may be formed of TaN or TiN.

[0019] Then, the wafer 10 is placed into a reactor and is preheated to 200°C or over 200°C. The reactor can be any type of plasma reactors, such as the parallel plate, the reactive ion etcher (RIE), the inductively coupled plasma (ICP), or the electron cyclotron resonance etcher (ECR), and the preheating procedure can utilize a lamp tray or a non-reactive gas plasma to preheat the wafer 10.

[0020] After the wafer 10 is preheated to 200°C or over 200°C, the bromine-rich gas plasma is supplied into the reactor

to remove portions of the HfO2-containing gate dielectric 12. The bromine-rich gas plasma can be a Br2 plasma, a HBr plasma, or a mixture of a Br2 plasma and a HBr plasma, and concentration of the bromine-rich gas plasma is higher than 30%. On the wafer surface, the bromine-rich gas plasma will react with the HfO2-containing gate dielectric 12 and produce a volatile product HfBr4. At the elevated temperature (≥200°C), HfBr4 is volatile and can be taken out by the pumping system. After removing portions of the HfO2-containing gate dielectric 12, the STI layer 18 is exposed. Since the bromine-rich gas plasma etches the SiO2 material of the STI layer 18 much slower than the HfO2-containing gate dielectric 12, the STI layer 18 will be almost undamaged. In addition, a sacrifice layer (not shown) can be further formed on the gate electrode 16 before performing the patterning process to protect the gate electrode 16. The sacrifice layer may be formed of SiO2.

[0021] Furthermore, in other embodiments of the present invention, additive gases, such as Ar, N2, He, O2, CHF3, etc., can be introduced into the reactor to assist uniform etching of the HfO2-containing gate dielectric 12. It is also worthy of notice that the present invention is not limited

to pattern the HfO2-containing gate dielectric. The present invention is also applicable in any etching process relating to pattern HfO2-containing dielectric. For example, a wafer having an HfO2-containing dielectric is provided, and the wafer is preheated to a predetermined temperature. Following that, a bromine-rich gas plasma is provided to remove portions of the HfO2-containing dielectric, thus providing a high etching selectivity in etching HfO2.

[0022] Another embodiment of the present invention is utilizing a nitrogen ion bombardment to convert the exposed HfO2-containing dielectric to an Hf3N4 (Hafnium Nitride) layer and then utilizing a phosphoric acid to remove the Hf3N4 layer. Please refer to Fig. 4, which shows the patterning process of the second embodiment. A nitrogen ion bombardment is performed on the half-manufactured wafer 10, and the exposed HfO2-containing gate dielectric 12 is converted to an Hf3N4 layer 20. While performing the nitrogen ion bombardment, a nitrogen gas or a nitrogen-contained gas can be used to produce the nitrogen ions. The regions covered by the gate electrode 16 and the spacers 14 are protected and retain the HfO2-containing material. Selectively, a sacrifice layer (not

shown) can be also formed on the gate electrode 16 before performing the nitrogen ion bombardment to protect the gate electrode 16.

[0023] After the nitrogen ion bombardment, the Hf_3N_4 layers 20 are formed beside the portion of HfO_2-containing gate dielectrics 12 under the gate electrode 16 and the spacers 14. The Hf_3N_4 layers 20 are easily etched by the phosphoric acid. In this embodiment, a H_3PO_4 solution is utilized to remove the Hf_3N_4 layers 20, but the H_3PO_4 solution etches neither the SiO_2 layer nor the Si layer. The STI layers 18 will be almost undamaged after the Hf_3N_4 layers 20 is removed. In addition, for speeding the removing process, the H_3PO_4 solution can be maintained at the temperature 50°C-300°C. It is also worthy of notice that the present invention is not limited to pattern the HfO_2-containing gate dielectric. The present invention is also applicable in any etching process relating to pattern HfO_2-containing dielectric. For example, a wafer having an HfO_2-containing dielectric is provided, and a nitrogen ion bombardment is used to convert portions of the HfO_2-containing dielectric to an Hf_3N_4 layer. Following that, a phosphoric acid is used to remove the Hf_3N_4 layer, thus providing a high etching selectivity in etching HfO_2.

[0024] In contrast to the prior art, the present invention has a high etching selectivity between the HfO2-containing material and the SiO2 material, so that the STI layer can be retained complete after the gate dielectric is removed.

[0025] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.